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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,171	02/16/2004	Wen-Chin Lin	24061.163 (TSMC2003.0276)	1738

42717 7590 11/01/2005

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SOFOCLEOUS, ALEXANDER	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,171	LIN ET AL.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *(1) 5/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 16, 2004, and the Information Disclosure Statement filed on May 27, 2004.

2. Claims 1-25 are pending in the case. Claims 1, 10, 15, 17, 18, and 25 are independent claims.

Specification

4. Paragraph 0021 indicates, "The free layer **14** is in contact with the second layer **12**." Layer "**12**" has previously been identified as the pinned layer. Examiner assumes that applicant intended for the second layer to be labeled "**15**."

5. Paragraph 0021 also indicates, "If the magnetization directions of the pinned layer 12 and the free layer 14 are not parallel, then the MTJ cell is storing a **first** binary digit, for example, '1'." Examiner assumes that applicant intended for this binary digit to be referred to as "**second**."

Appropriate correction is required.

Drawings

6. Figures 1A, 1B, 1C, 2A, 2B, and 3 should be designated by a legend such as -- Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should

be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claim 1-9, 15-16, 18-23, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Okazawa U.S. Patent Application Publication No. 2002/0034117A1.**

Regarding independent claim 1, Okazawa shows an MRAM memory array (Fig. 4 [1]) that comprises: a global word line (Fig. 4 [BSL1]), a global bit line (Fig. 4 [WSL1]), a plurality of word lines crossing the global bit line (Fig. 4 [MW1, MWm]), a plurality of bit lines crossing the global word line (Fig. 4 [MB1, MBn), a plurality of first switches that are coupled to the global word line and one or more bit lines (Fig. 4 [BT1, BTn]), a plurality of second switches that are coupled to the global bit line and one or more word lines (Fig. 4 [WT11, WT1m]), a plurality of memory cells (Fig. 4 [C]) that are magnetic tunnel junction, or MTJ, devices (Paragraph 0011) including: a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). Each of the plurality of MTJ cells are

positioned at crossing points of a bit line and a word line; and each of the MTJ cells is connected between the switch at the corresponding crossing bit line and the switch at the corresponding crossing word line (see Fig. 4).

Regarding dependent claim 2, Okazawa shows that the total number of switches is equal to the total number of plurality of word lines and the plurality of bit lines (see Fig. 4).

Regarding dependent claim 3, Okazawa shows that the total number of MTJ memories is equal to the product of the number of plurality of word lines and the number of plurality of bit lines (see Fig. 4).

Regarding dependent claim 4, Okazawa shows the first switch (Fig. 4 [BT11]) that includes: a first terminal (Fig. 4 [connection from BT11 to SB11]), a control gate coupled to the global word line (Fig. 4 [connection from BT11 to BSL1]), and a second terminal coupled to the corresponding bit line (Fig. 4 [connection from BT11 to MB1]).

Regarding dependent claim 5, Okazawa shows the second switch (Fig. 4 [WT11]) that includes: a first terminal (Fig. 4 [connection from WT11 to SW11]), a control gate coupled to the global bit line (Fig. 4 [connection from WT11 to WSL1]), and a second terminal coupled to the corresponding word line (Fig. 4 [connection from WT11 to MW1]).

Regarding dependent claim 6, Okazawa shows magnetic tunnel junction memory being connected between the first terminal of the first switch (Fig. 4 [connection from BT11 to SB11]) and the first terminal of the second switch (Fig. 4 [connection from WT11 to SW11]).

Regarding dependent claim 7, Okazawa shows that the switches are NMOS transistors (see Fig. 4 [BT11, WT11]).

Regarding dependent claim 8 and 9, Okazawa teaches that the memory array is an "m" x "n" matrix array (paragraph 0068), which denotes implicit variability of array dimensions; hence the 2 bit lines x 3 word lines and 3 bit lines x 3 word lines arrays are anticipated.

Regarding independent claim 15, Okazawa shows a MRAM array that comprises a global word line (Fig. 4 [BSL1]), a global bit line (Fig. 4 [WSL1]), a first word line (Fig. 4 [MW1]), a second word line (Fig. 4 [MWm]), and a third word line (Fig. 4 [MWm]). Okazawa shows a first bit line that crosses the first word line and the second word line and the third word line (Fig. 4 [MB1]), and a second bit line that crosses the first word line and the second word line and the third word line (Fig. 4 [MBn]). The "m" and "n" denote implicit variability of array dimensions (as discussed supra with respect to claims 8-9); hence the 2 bit lines x 3 word lines array is anticipated.

Okazawa shows a first switch (Fig. 4 [BT11]) having a first terminal (Fig. 4 [connection from BT11 to SB11]), a second terminal connected to the first bit line (Fig. 4 [connection from BT11 to MB1), and a control gate connected to the global word line (Fig. 4 [connection from BT11 to BSL1]).

Okazawa shows a second switch (Fig. 4 [BT1n]) having a first terminal (Fig. 4 [connection from BT1n to SB1n]), a second terminal connected to the second bit line (Fig. 4 [connection from BT1n to MBn), and a control gate connected to the global word line (Fig. 4 [connection from BT1n to BSL1]).

Okazawa shows a third switch (Fig. 4 [WT11]) having a first terminal (Fig. 4 [connection from WT11 to SW11]), a second terminal connected to the first word line (Fig. 4 [connection from WT11 to MW1), and a control gate connected to the global bit line (Fig. 4 [connection from WT11 to WSL1]).

Okazawa shows a fourth switch (Fig. 4 [WT1n]) having a first terminal (Fig. 4 [connection from WT1n to SW1n]), a second terminal connected to the second word line (Fig. 4 [connection from WT1n to MWn), and a control gate connected to the global bit line (Fig. 4 [connection from WT1n to WSL1]).

Okazawa shows a fifth switch (Fig. 4 [WT1n]) having a first terminal (Fig. 4 [connection from WT1n to SW1n]), a second terminal connected to the third word line (Fig. 4 [connection from WT1n to MWn), and a control gate connected to the global bit line (Fig. 4 [connection from WT1n to WSL1]).

The first MTJ memory cell (Fig. 4 [C selected by BT11 and WT11]) is connected between the first switch's first terminal and the third switch's first terminal. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the first bit line (Fig. 4 [MB1]) and the first word line (Fig. 4 [MW1]).

The second MTJ memory cell (Fig. 4 [C selected by BT1n and WT11]) is connected between the second switch's first terminal and the third switch's first terminal. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This

MTJ is positioned at the cross-point of the second bit line (Fig. 4 [MBn]) and the first word line (Fig. 4 [MW1]).

The third MTJ memory cell (Fig. 4 [C selected by BT11 and WT1m]) is connected between the first switch's first terminal and the fourth switch's first terminal. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the first bit line (Fig. 4 [MB1]) and the second word line (Fig. 4 [MWm]).

The fourth MTJ memory cell (Fig. 4 [C selected by BT1n and WT1m]) is connected between the second switch's first terminal and the fourth switch's first terminal. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the second bit line (Fig. 4 [MBn]) and the second word line (Fig. 4 [MWm]).

The fifth MTJ memory cell (Fig. 4 [C selected by BT11 and WT1m]) is connected between the first switch's first terminal and the fifth switch's first terminal. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the first bit line (Fig. 4 [MB1]) and the third word line (Fig. 4 [MWm]).

The sixth MTJ memory cell (Fig. 4 [C selected by BT1n and WT1m]) is connected between the second switch's first terminal and the fifth switch's first terminal.

The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the second bit line (Fig. 4 [MBn]) and the third word line (Fig. 4 [MWm]).

Regarding dependent claim 16, Okazawa shows that the switches are NMOS transistors (see Fig. 4 [BT11, BTn, WT11, WT1m]).

Regarding independent claim 18, Okazawa shows a first bus (Fig. 4 [BSL1]) associated with a plurality of first conductive lines (Fig. 4 [MW1, MWm]) and a second bus (Fig. 4 [WSL1]) associated with a plurality of second conductive lines (Fig. 4 [MB1, MBn]).

A plurality of first switches (Fig. 4 [BT11, BT1n]) couples the first bus (Fig. 4 [BSL1]) to the second conductive lines (Fig. 4 [MB1, MBn]) and a plurality of second switches (Fig. 4 [WT11, WT1m]) connects the second bus (Fig. 4 [WSL1]) to the first conductive lines (Fig. 4 [MW1, MWm]).

A plurality of magnetic tunnel junction memories (Fig. 4 [C]) are positioned where one first conductive line and one second conductive line crosses (see Fig. 4 [MW1 and MB1]) wherein each of the plurality of MJT memories is connected between a first switch (see Fig. 4 [BT11]) at a corresponding second conductive line (see Fig. 4 [MB1]) and a second switch (see Fig. 4 [WT11]) at a corresponding first conductive line (see Fig. 4 [MW1]).

As per **claim 25**, it encompasses the same scope of invention as to that of claim 18 except it drafts in method of manufacture format instead of apparatus format. The claim is therefore rejected for the same reasons as set forth above.

Regarding independent claim 19, each of the MJT memories includes a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]).

Regarding dependent claim 20, Okazawa shows that the total number of first and second switches is equal to the total number of plurality of first and second conductive lines (see Fig. 4).

Regarding dependent claim 21, Okazawa shows that the total number of MJT cells is equal to the product of the number of plurality of first conduction lines and the number of plurality of second conductive lines (see Fig. 4).

Regarding independent claim 22, Okazawa shows a plurality of segments (Fig. 4 [SW11, SW1m, SB11, SB1n]), wherein each segment includes at least two of the plurality of MTJ memories (see Fig. 4).

Regarding independent claim 23, Okazawa shows a plurality of segments (Fig. 4 [SW11, SW1m, SB11, SB1n]) that are separated by field effect transistors (Fig. 4 [WT11, WT1m, BT11, BT1n]).

9. **Claims 10-14, 17, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Okazawa U.S. Patent Application Publication No. 2002/0034117A1 as supported by Tran U.S. Patent 6,356,477B1.**

Regarding independent claim 10, Okazawa shows word lines (Fig. 4 MW1, MWm]), bit lines crossing the word lines (Fig. 4 [MB1, MBn]), a first set of switches coupled to the corresponding bit line (Fig. 4 [BT11]), a second set of switches coupled to the corresponding word line (Fig. 4 [WT11]), and memory cells (Fig. 4 [C]) that are magnetic tunnel junction, or MTJ, devices (Paragraph 0011) including: a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]).

Although Okazawa is silent with respect to the specific provision of diodes in the circuit as replacements for the transistors, it is inherent that the source to drain of such transistor will effectively function as a diode (e.g., intrinsic diode). Tran further supports the fact that transistors having intrinsic diodes can be replaced by diodes for the purposes of blocking sneak/reverse currents in memory arrays (see Tran Fig. 10 with respect to Tran Fig. 4; Tran column 2, lines 50-52; Tran column 5, lines 16-20).

Each of the plurality of MTJ cells are positioned at crossing points of a bit line and a word line; and each of the MTJ cells is connected between the switch at the corresponding crossing bit line and the switch at the corresponding crossing word line (see Fig. 4).

Regarding dependent claim 11, Okazawa shows that the total number of diodes (as discussed supra with respect to claim 10) is equal to the total number of plurality of word lines and the plurality of bit lines (see Fig. 4).

Regarding dependent claim 12, Okazawa shows that the total number of cells is equal to the number of plurality of word lines times the number of plurality of bit lines (see Fig. 4).

Regarding dependent claim 13 and 14, Okazawa teaches that the memory array is an "m" x "n" matrix array, which denotes implicit variability of array dimensions (as discussed supra with respect to claims 8-9); hence 2 bit lines x 3 word lines and 3 bit lines x 3 word lines arrays are anticipated.

Regarding independent claim 17, Okazawa shows a MRAM array that comprises a first word line (Fig. 4 [MW1]), a second word line (Fig. 4 [MWm]), and a third word line (Fig. 4 [MWm]). Okazawa shows a first bit line that crosses the first word line and the second word line and the third word line (Fig. 4 [MB1]), and a second bit line that crosses the first word line and the second word line and the third word line (Fig. 4 [MBn]). The "m" and "n" denote implicit variability of array dimensions (as discussed supra with respect to claims 8-9); hence, the 2 bit lines x 3 word lines array is anticipated.

Although Okazawa is silent with respect the specific provision of diodes in the circuit as replacements for the transistors, it is inherent that the source to drain of the NMOS transistor effectively functions as a diode (e.g., intrinsic diode; as discussed supra with respect to claim 10). For the diodes coupled to the bit lines, the anode is connected to the bit line and the cathode is connected to the memory cell. For the diodes coupled to the word line, the anode is connected to the memory cell and the anode is connected to the word line. Tran further supports the fact that transistors

having intrinsic diodes can be replaced by diodes for the purpose of blocking sneak currents in memory arrays and such that the current is only conducted by the memory elements connected to the selected bit lines (see Tran Fig. 10 with respect to Tran Fig. 4; and Tran column 4 lines 3-5). Therefore, the first diode's anode is coupled to the first bit line is shown (Fig. 4 [BT11]) and the first diode's cathode is coupled to a memory cell; and the second diode's anode is coupled to the second bit line (Fig. 4 [BT1n]) and the second diode's cathode is coupled to a memory cell.

Furthermore, the third diode's cathode is coupled to the first word line (Fig. 4 [WT11]) and the third diode's anode is coupled to a memory cell; the fourth diode's cathode is coupled to the second word line (Fig. 4 [WT1m]) and the fourth diode's anode is coupled to a memory cell; and the fifth diode's cathode is coupled to the third word line (Fig. 4 [WT1m]) and the fifth diode's anode is coupled to a memory cell.

The first MTJ memory cell (Fig. 4 [C selected by BT11 and WT11]) is connected between the first diode's cathode and the third diode's anode. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the first bit line (Fig. 4 [MB1]) and the first word line (Fig. 4 [MW1]).

The second MTJ memory cell (Fig. 4 [C selected by BT1n and WT11]) is connected between the second diode's cathode and the third diode's anode. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is

positioned at the cross-point of the second bit line (Fig. 4 [MBn]) and the first word line (Fig. 4 [MW1]).

The third MTJ memory cell (Fig. 4 [C selected by BT11 and WT1m]) is connected between the first diode's cathode and the fourth diode's anode. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the first bit line (Fig. 4 [MB1]) and the second word line (Fig. 4 [MWm]).

The fourth MTJ memory cell (Fig. 4 [C selected by BT1n and WT1m]) is connected between the second diode's cathode and the fourth diode's anode. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the second bit line (Fig. 4 [MBn]) and the second word line (Fig. 4 [MWm]).

The fifth MTJ memory cell (Fig. 4 [C selected by BT11 and WT1m]) is connected between the first diode's cathode and the fifth diode's anode. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is positioned at the cross-point of the first bit line (Fig. 4 [MB1]) and the third word line (Fig. 4 [MWm]).

The sixth MTJ memory cell (Fig. 4 [C selected by BT1n and WT1m]) is connected between the second diode's cathode and the fifth diode's anode. The MTJ has a pinned layer (Fig. 1A [12]), a free layer (Fig. 1A [14]), and a non-magnetic layer located between the pinned layer and the free layer (Fig. 1A [13]). This MTJ is

positioned at the cross-point of the second bit line (Fig. 4 [MBn]) and the third word line (Fig. 4 [MWm]).

Regarding dependent claim 24, Okazawa shows the segments (Fig. 4 [SW31, SW3m]) are separated by diodes (as discussed supra with respect to claim 10)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Silvagni et al. U.S. Patent 6,891,755B2, Tsang U.S. Patent 6,870,759B2, and DeBrosse et al. U.S. Patent 6,490,217B1.

Silvagni et al. shows a cross-point array with main word lines and main bit lines that are selected by switches. Tsang shows an MRAM cross-point array with global word lines. DeBrosse et al. shows a segmented MRAM cross-point array.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

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